EXHIBIT 3

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC., Defendant.	)	C.A. No. 13-cv-1835-RGA PUBLIC VERSION FILED JUNE 27, 2019

DEFENDANT 2WIRE, INC.'S OPENING BRIEF IN SUPPORT OF ITS MOTION FOR JUDGMENT AS A MATTER OF LAW, OR, IN THE ALTERNATIVE, FOR A NEW TRIAL FOR FAMILY 3

Dated: June 20, 2019

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I. INTRODUCTION

The Court should grant judgment as a matter of law ("JMOL") that (1) 2Wire does not infringe the asserted claims and (2) the asserted claims are invalid as obvious over the prior art.[1] TQ Delta failed to provide substantial evidence to support the jury's verdict on these issues and, thus, JMOL is appropriate. In the alternative, 2Wire requests a new trial on these issues.

With respect to infringement, JMOL is appropriate because TQ Delta failed to provide substantial evidence that the accused 2Wire products satisfy three limitations required by every asserted claim. *First*, no reasonable jury could have found that the accused products transmit or receive "a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to" an interleaver or deinterleaver. For this limitation, TQ Delta relied upon the value of max_delay_octet / 2. But max_delay_octet / 2 is the *minimum* amount of memory—not the maximum—required to support the maximum end-to-end delay, as the VDSL2 standard itself states. Moreover, TQ Delta's infringement theory failed to address the "maximum" claim language at all: TQ Delta's expert, Dr. Cooklev, testified only that the amount of memory "actually being used" by the interleaver on the central office side and the deinterleaver on the customer side must be equal to max_delay_octet / 2. *See* Trial Tr., at p. 270:6–13 (Cooklev). But the claims do not require a message specifying the amount of memory "actually being used"; instead, the claimed message must specify "a maximum number of bytes of memory that are ***available to be allocated*** to" an interleaver or deinterleaver.

Second, no reasonable jury could have found that the accused 2Wire products meet the limitation "determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory," or the

[1] The asserted claims are claim 1 of U.S. Patent No. 8,276,048 (the "'048 patent") (JTX-0003), claim 5 of U.S. Patent No. 7,836,381 (the "'381 patent") (JTX-0001), and claim 13 of U.S. Patent No. 7,844,882 (the "'882 patent") (JTX-0002).

corresponding limitation in the '048 patent directed to determining an amount of memory for the interleaver. For this limitation, TQ Delta relied on a formula, (D – 1) x (I – 1) / 2, set forth in the VDSL2 standard. But TQ Delta's expert admitted that the Broadcom chips that are used by the accused products use different formulas to determine the amount of memory required, and a Broadcom witness, Dr. Gong-San Yu, testified at trial that none of the accused products use the (D – 1) x (I – 1) / 2 formula to determine interleaver or deinterleaver memory.

Third, no reasonable jury could find that the accused products satisfy the requirement that "the allocated memory for the deinterleaver [or interleaver] does not exceed the maximum number of bytes specified in the message." At first, Dr. Cooklev testified that the amount of memory allocated to the interleaver or deinterleaver in the accused products does not exceed the value of max_delay_octet / 2, as used in VDSL2. However, when pressed about whether the Broadcom DSL chips actually allocate memory to the interleaver or deinterleaver in an amount greater than max_delay_octet / 2, Dr. Cooklev testified that the accused products "might not always operate in a way specified by the [VDSL2] standard"; instead, Dr. Cooklev admitted, "there is a Broadcom proprietary way in which they operate." Trial Tr., at pp. 390:22–391:2 (Cooklev). The jury then heard about the "Broadcom proprietary way" from Dr. Yu, who heads the development of Broadcom's DSL CPE chips. Dr. Yu testified that, for both the accused BCM6091 and BCM63x68 chips, [redacted] *Id.*, at pp. 720:23–721:3, 729:19–24 (Yu). No reasonable jury could find, in light of this testimony, that the allocated memory for the interleaver or the deinterleaver does not exceed max_delay_octet / 2. Dr. Yu's undisputed testimony alone warrants granting JMOL of non-infringement.

Faced with that undisputed testimony, TQ Delta was forced to argue that any memory required for interleaving or deinterleaving beyond the value of max_delay_octet / 2 is merely

"peripheral memory," and not "interleaver memory" or "deinterleaver memory." To get here, TQ Delta invented a heretofore unseen and unsupported construction into the claim language—that interleaver/deinterleaver memory is only the memory required to hold Reed-Solomon coded data, no more and no less. But TQ Delta's attempt to explain away the "memory" above the supposed maximum was not based on the actual claim language, which does not distinguish "interleaver memory" or "deinterleaver memory" from any other "memory." And even if it did, all parties, including TQ Delta's own expert, Dr. Cooklev, agreed that what TQ Delta dismissed as "peripheral memory" is required to perform the interleaving and deinterleaving functions. Moreover, Dr. Cooklev never explains how, in the face of testimony from Broadcom's Dr. Yu to the contrary, the interleaver and deinterleaver could function by using the minimum, theoretical amount of memory he proposes. *See* Trial Tr., at pp. 728:12–729:18 (Dr. Yu explaining [redacted]. Therefore, the evidence conclusively establishes that the allocated memory for the deinterleaver or interleaver exceeds max_delay_octet / 2 in both Broadcom chips at issue in the case.

With respect to invalidity, the Court should grant JMOL that the asserted claims are invalid as obvious based on LB-031 (JTX-0057) as understood by a person of ordinary skill in the art ("POSITA") or LB-031 in combination with Mazzoni (JTX-0056). At trial, TQ Delta challenged only whether the LB-031 messaging scheme could be used with shared memory. Dr. Jacobsen explained that there are only two types of memory to be used in a transceiver, dedicated memory and shared memory, and, thus, a POSITA reading LB-031 "would have understood it to apply to either kind of [memory] implementation." Trial Tr., at p. 630:7–10 (Jacobsen). As to the combination of LB-031 and Mazzoni, TQ Delta raised the alleged "Mazzoni problem," but Dr. Jacobsen explained that a POSITA would not recognize that as a problem at all, and, in any event, the problem could be solved to allow for the advantages of the

LB-031 messaging scheme for use with shared memory. *Id.*, at pp. 645:4–646:12, 676:20–24.

Accordingly, 2Wire respectfully requests that the Court grant JMOL of non-infringement and invalidity of all asserted claims. In the alternative, 2Wire respectfully submits that, for the same reasons, the Court should grant a new trial on infringement and invalidity.

II. LEGAL STANDARD

JMOL is required if "the court finds that a reasonable jury would not have a legally sufficient evidentiary basis to find for [a] party." Fed. R. Civ. P. 50(a)(1). "To prevail on a renewed motion for JMOL following a jury trial, a party 'must show that the jury's findings, presumed or express, are not supported by substantial evidence or, if they were, that the legal conclusion(s) implied [by] the jury's verdict cannot in law be supported by those findings.'" *Pannu v. Iolab Corp.*, 155 F.3d 1344, 1348 (Fed. Cir. 1998).

Under Rule 59(a), "[t]he court may, on motion, grant a new trial on all or some of the issues—and to any party— . . . after a jury trial, for any reason for which a new trial has heretofore been granted in an action at law in federal court . . . ." Fed. R. Civ. P. 59(a)(1)(A). Among the most common grounds for granting a new trial is when "the jury's verdict is against the clear weight of the evidence, and a new trial must be granted to prevent a miscarriage of justice . . . ." *AVM Techs., LLC v. Intel Corp.*, 334 F. Supp. 3d 623, 626 (D. Del. 2018). "The decision to grant or deny a new trial is within the sound discretion of the trial court and, unlike the standard for determining judgment as a matter of law, the court need not view the evidence in the light most favorable to the verdict winner." *Carrier Corp. v. Goodman Glob., Inc.*, 162 F. Supp. 3d 345, 351 (D. Del. 2016) (citations omitted).

III. ARGUMENT

A. The Court Should Enter JMOL That 2Wire Does Not Infringe the Asserted Claims.

1. No Reasonable Jury Could Find That The Accused Products Satisfy The "Transmitting Or Receiving A Message" Limitation.

On the evidence presented at trial, no reasonable jury could find that the accused products satisfy the step of "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated" to an interleaver or a deinterleaver. TQ Delta argued that this limitation was satisfied based upon the calculation of max_delay_octet / 2, as derived from the O-PMS message parameters. *See, e.g.*, Trial Tr., at 269:11–13 (Cooklev); PTX-505 (Cooklev Direct Demonstratives), at p. 82. The value of max_delay_octet / 2 does not satisfy this claim limitation because it is not a maximum value of memory at all, much less a maximum amount of ***available*** memory.[2]

Under the VDSL2 standard itself, max_delay_octet does not specify "a maximum number of bytes of memory that are available to be allocated" to an interleaver or a deinterleaver. Rather, max_delay_octet specifies the maximum end-to-end ***delay*** on a particular latency path. *See* JTX-0040, at p. 254 (VDSL2, at § 12.3.5.2.1.3: describing field #8 max_delay $octet_{DS,0}$ and field #9 max_delay $octet_{US,0}$). As Dr. Jacobsen and Dr. Yu testified, specifying a

[2] In its April 25, 2019 Memorandum Opinion, the Court denied summary judgment of non-infringement, finding that a dispute of material fact existed as to the "message" limitation because, "[i]f, as Plaintiff contends, the message sent during initialization functions as a maximum then it may meet the requirement of the claim—despite being labeled as a minimum in the standard." D.I. 1106, at pp. 13–14. As discussed in Section III.A.3, *infra*, the undisputed evidence at trial established that the accused products do in fact allocate more memory to the interleaver and the deinterleaver than the value of max_delay_octet / 2. The max_delay_octet parameters in the O-PMS message thus do not function as a maximum, and this limitation is not met by the accused products. And even TQ Delta's interpretation of the claims fails, as it stretches the meaning of the term "maximum amount of memory" so far as to mean a minimum. TQ Delta's arguments can be rejected on that basis alone.

maximum amount of **delay** is not the same as specifying a maximum amount of **memory**. *See* Trial Tr., at p. 613:17–614:25, 608:4–609:12 (Jacobsen); *id.*, at pp. 718:15–719:1 (Yu) [redacted].

Furthermore, the VDSL2 standard provides that the actual end-to-end delay, which depends on the selected parameters, is denoted as delay_octet; as the name suggests, max_delay_octet specifies the maximum value of delay_octet. According to the standard, the ***minimum amount*** of memory each transceiver must provide to support the actual end-to-end delay of delay_octet is half of the value of the actual end-to-end delay, or delay_octet / 2. *See* JTX-0040, at p. 33 (VDSL2, at § 6.2.8: "Each interleaver and each de-interleaver for each latency path requires ***at least*** ($delay\_octet_{x,p}/2$) octets of memory to meet this delay.") (emphasis added); *see also* Trial Tr., at p. 614:7–8 (Jacobsen) ("So what the delay specifies is a minimum amount of memory that needs to be allocated."). As Dr. Jacobsen testified, specifying a **minimum** amount of memory is not the same as specifying a **maximum** amount of memory. *See, e.g.*, Trial Tr., at p. 624:2–6 ("[T]he max_delay_octet values can affect the minimum amounts of memory, but they don't establish a maximum. And it's because of the fact that the minimum amount of memory required to meet the delay is part of the delay value.").

Despite the plain language of the VDSL2 standard, Dr. Cooklev attempted to explain why he believed that max_delay_octet / 2 nevertheless satisfied the "message" claim limitation. His explanation focused on the amount of memory "actually being used" by the interleaver and the deinterleaver, which, according to him, each had to be equal to max_delay_octet / 2:

> Q. Now, yesterday we all heard that 2Wire plans to argue that the max_delay_octet O-PMS message is a minimum and not a maximum. Do you agree with that conclusion?

A. No, I disagree with that. 2Wire is trying to confuse the members of the jury.

Q. Why is that your opinion?

A. Well, I will give a simple example using the figure on the slide [slide 60 of PTX-505]. So the figure, and let me remind everyone where we were when we left off yesterday. The figure on the slide shows a central office transceiver on the left and a CPE transceiver on the right. And furthermore, it shows that in orange here at the central office transceiver is the deinterleaver memory. Also in orange at the CPE transceiver is the interleaver memory.

It is critically important that the amount of the [de]interleaver memory at the central office transceiver, again, that's in orange, it's critically important that that amount is **exactly the same as the amount of interleaver memory at the CPE transceiver <u>actually being used</u>** as shown on this figure.

In the upstream direction with blue at the CPE transceiver is the amount of interleaver memory actually being used. Excuse me, the deinterleaver memory at the CPE transceiver **<u>actually being used</u>**.

And with blue at the central office transceiver is the corresponding amount of memory. **It is critically important that these amounts are identical. And each one is equal to max_delay_octet divided by two.**

Id., at pp. 269:11–270:13 (emphasis added); PTX-505 (Cooklev Direct Demonstratives), at p. 60.

Even taking Dr. Cooklev's testimony to be true, the asserted claims do not recite anywhere that the claimed "message" specifies an amount of memory "actually being used" by the interleaver or deinterleaver. Rather, the claims all require a message that specifies "a maximum number of bytes of memory that are ***available to be allocated***" to the interleaver or deinterleaver. With respect to the actual claim language—that is, the amount of memory "available to be allocated"—Dr. Cooklev admitted that the amount of memory available to be allocated at the central office and at the customer premises do not need to be identical; rather, he testified, the amount of memory available could be more than what is specified in the message:

[Q.] So it's interesting, I think something may have just occurred to me. You keep talking about ***the memory that is used*** needs to be the same. Do I understand that correctly?

A. Yes.

Q. But the memory that's available doesn't need to be the same; isn't that right? It's okay if somebody has available more memory than they need; correct?

A. That's correct.

Trial Tr., at pp. 359:24–360:7 (Cooklev) (emphasis added); *see also id.*, at p. 358:9–17 ("Q. If they have more memory than they need, that doesn't break the system; isn't that right? A. That's correct.").

Accordingly, TQ Delta failed to provide substantial evidence to support the jury's finding that the accused products satisfy the step of "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated" to an interleaver or a deinterleaver.[3]

2. No Reasonable Jury Could Find That The Accused Products Satisfy The "Determining" Limitation.

On the evidence presented at trial, no reasonable jury could find that the accused 2Wire products satisfy the limitation requiring "determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory," in claim 13 of the '882 patent and claim 5 of the '381 patent, and "determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory," in claim 1 of the '048 patent. TQ Delta's evidence fails here for two reasons: (1) the accused products do not perform the "determining" step in the manner claimed by TQ Delta; and (2) TQ Delta's theory of "determining" ignores all of the memory "required by the interleaver to interleave" and all of the memory "required by the deinterleaver to deinterleave."

First, TQ Delta and Dr. Cooklev argued at trial that the "determining" limitations are met

[3] At no point did TQ Delta identify anything besides max_delay_octet / 2 that would meet this limitation.

by the accused products through the calculation of (D – 1) x (I – 1) / 2, as specified in the VDSL2 standard. *See* Trial Tr., at pp. 305:12–15 (Cooklev) ("And with the formula in the standard, I minus one times D minus one over two, that I think I explained that formula yesterday. So we can calculate the amount of deinterleaver memory actually used by the CPE transceiver."); *id.*, at pp. 334:12–335:9 (discussing, for the "determining" limitation of claim 1 of the '048 patent, "[t]he I and D in the O-PMS message which specify the interleaver parameters that the CPE transceiver must use"). However, it is undisputed that that is not how the Broadcom DSL chipsets determine the amount of memory required by the interleaver or the deinterleaver. When confronted with one of the Broadcom formulas that was not simply (D – 1) x (I – 1) / 2, Dr. Cooklev conceded that "the products might not always operate in a way specified by the standard" because "there is a Broadcom proprietary way in which they operate." *Id.*, at pp. 390:25–391:2 (Cooklev).

Broadcom's Dr. Yu testified regarding the proprietary formulas used by the Broadcom DSL chips to calculate the amount of memory required by the interleaver or deinterleaver. He testified that neither of the chips use the formula (D – 1) x (I – 1) / 2. For example, Dr. Yu testified that, for the BCM6091 chip, the amount of memory required for the interleaver is calculated using the formula [redacted] *See* JTX-0087, at p. 2 (lines 3270–71); Trial Tr., at p. 717:17–23 (Yu) (stating: [redacted]; *see also id.*, at pp. 467:23–468:23 (Dr. Almeroth confirming calculation). The amount of memory required for the deinterleaver is calculated by [redacted] *See id.*, at pp. 719:24–720:7.

For chipsets using the BCM63x68 source code, Dr. Yu testified that the amount of

memory required for the interleaver is determined by [redacted] *See* Trial Tr., at p. 724:17–20 (Yu) [redacted] For the deinterleaver side, Dr. Yu similarly testified that the amount of memory actually allocated to the deinterleaver in the BCM63x68 source code is [redacted] *Id.*, at p. 729:19–24 [redacted]

Second, TQ Delta's reliance upon (D – 1) x (I – 1) / 2 for the "determining" step explicitly fails to take into account memory that is determined by the Broadcom chips using the formulas and that is actually required to perform interleaving and deinterleaving. Dr. Cooklev attempted to dismiss this additional memory from the relevant calculation on the grounds that "any additional peripheral memory is not used to store Reed-Solomon coded data bytes for the purpose of delaying them." *Id.*, at p. 307:20–22. As elsewhere, TQ Delta's argument is not based on language set forth in any of the asserted claims. The claims do not limit the determined amount of memory to only that memory "used to store Reed-Solomon coded data bytes for the purpose of delaying them." Rather, the claims require "determining an amount of memory ***required by the deinterleaver to deinterleave*** a first plurality of Reed Solomon (RS) coded data bytes within a shared memory." It is undisputed that the so-called "overhead" or "peripheral memory" that TQ Delta dismissed at trial is ***required*** by the Broadcom DSL chips to perform interleaving and deinterleaving. Dr. Yu and Dr. Cooklev both testified to this:

Dr. Yu	Dr. Cooklev
[redacted] *Id.*, at p. 728:13–16. [redacted] *Id.*, at p. 730:3–5. *See also id.*, at pp. 728:18–729:15 [redacted]	Q. The Z bytes of memory which is the additional memory that the interleaver or deinterleaver function needs to interleave the Reed Solomon coded bytes are not included in the O-PMS message; isn't that correct? A. Additional memory is not needed to be included. Q. But it is not included in the O-PMS message? A. Yes, it is not included. Q. Yet it is needed to interleave the Reed Solomon coded bytes; correct? A. It may be needed, yes. *Id.*, at p. 369:16–25.

This evidence establishes that the accused products do not determine "an amount of memory required by the interleaver to interleave" or "an amount of memory required by the deinterleaver to deinterleave" by simply applying the formula (D – 1) x (I – 1) / 2. Therefore, no reasonable jury could conclude that the accused products satisfy the "determining" step of the asserted claims in the way TQ Delta argued at trial.

3. No Reasonable Jury Could Find That The Accused Products Satisfy The First "Allocating" Limitation.

Each of the asserted claims has a first "allocating" step requiring that "the allocated memory for the deinterleaver [or interleaver] does not exceed the maximum number of bytes specified in the message." *See, e.g.*, '882 patent, claim 13. No reasonable jury, applying the plain and ordinary meaning of this claim language and the Court's constructions, could find that this limitation is met by any of the accused products.

The undisputed evidence at trial establishes that each of the Broadcom DSL chips at issue allocates memory for the interleaver and the deinterleaver in an amount greater than

max_delay_octet / 2, *i.e.*, the maximum amount of memory TQ Delta contends is specified by the allegedly infringing message. Broadcom's Dr. Yu confirmed this fact for the interleaver and the deinterleaver for both the BCM6091 and BCM63x68 source code:

BCM6091 Source Code	
Allocating memory for the interleaver	[redacted] *Id.*, at p. 719:14–20. *See id.*, at p. 721:17–23 (confirming that [redacted].
Allocating memory for the deinterleaver	[redacted] *Id.*, at p. 722:14–17. [redacted] *Id.*, at pp. 720:23–721:3.
BCM63x68 Source Code	
Allocating memory for the interleaver	[redacted] *Id.*, at pp. 727:25–728:11.
Allocating memory for the deinterleaver	[redacted]

	Id., at p. 729:19–24.

Consistent with Dr. Yu's knowledge and discussion of the operations of the Broadcom DSL chips, TQ Delta's source code expert, Dr. Almeroth, testified that, when considering ***all*** of the memory required for interleaving (or deinterleaving), the amount of memory allocated in the accused 2Wire products for the interleaver (or the deinterleaver) would exceed the specified value of max_delay_octet / 2:

> Q. So I'll phrase it in the form of a hypothetical for you, Dr. Almeroth. Assume I'm talking about memory, all of the memory that the BCM6091 allocates for what it calls interleaver memory. You would agree with me that using the formula that we have just been looking at in the Broadcom source code, interleaver memory can exceed the value received in the O-PMS message for the max_delay_octet upstream field?
>
> A. In your hypothetical, ***if you assume the definition of interleaver memory is not just limited to the depth and the width of the code word, but also includes the management information, then yes, it would exceed that value***.

Id., at p. 472:12–23 (Almeroth) (emphasis added). Thus, the total amount of memory allocated *does* exceed the (supposed) maximum amount specified in the allegedly infringing message.

Because it could not rebut Dr. Yu's testimony or Dr. Almeroth's concession, and despite the clear language of the claims, TQ Delta argued that some types of memory simply do not count: it sought to distinguish between "interleaver memory" or "deinterleaver memory," on the one hand, and "peripheral memory" required for pointers and addresses used during interleaving and deinterleaving, on the other. *See, e.g.*, *id.*, at pp. 307:4–16, 400:7–16 (Cooklev). But, TQ Delta's attempted distinction is irrelevant because the asserted claims require looking to the allocated "memory," not just "interleaver memory" or "deinterleaver memory"—terms that the asserted claims do not even use. And no reasonable jury could reject that what TQ Delta calls "peripheral memory" is "memory." That memory cannot be ignored merely because it is inconvenient to TQ Delta's infringement theory.

TQ Delta's evidence and arguments at trial contradict the claim language itself. Rather than discussing any "interleaver memory" or "deinterleaver memory," the asserted claims recite "allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave . . . , wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message." Nothing in the plain language of this "wherein" clause permits TQ Delta to simply disregard or dismiss a portion of the memory actually allocated to the deinterleaver and required to do deinterleaving and instead misleadingly focus on some lesser portion of the allocated memory that TQ Delta contends only stores Reed-Solomon coded information. The same holds true for the interleaver of claim 1 of the '048 patent. Indeed, the Court construed the term "amount of memory" to have its plain and ordinary meaning, and TQ Delta never sought any construction for "memory" that would support the infringement theory that TQ Delta deployed at trial. And, as already discussed above, both Dr. Yu and Dr. Cooklev acknowledged that the "peripheral memory" or "overhead" part of the allocated memory is required to perform the interleaving and deinterleaving functions. Thus, there is no basis to exclude such memory from the "allocated memory" in the "wherein" clause.

In light of the above, no reasonable jury applying the plain and ordinary meaning of the "wherein the allocated memory for the deinterleaver [or interleaver] does not exceed the maximum number of bytes specified in the message" clause could have found that any of the accused 2Wire products satisfy that requirement.

B. The Court Should Enter JMOL That The Asserted Claims Are Invalid As Obvious.

1. The Court Should Find The Asserted Claims Obvious In View Of LB-031 As Understood By A POSITA.

The Court should enter JMOL that the asserted claims are invalid as obvious in view of LB-031 as understood by a POSITA. At trial, TQ Delta did not dispute that each limitation of

the asserted claims was found in the prior art and only disputed whether a POSITA would have used the disclosures of LB-031 in conjunction with shared memory. *See* Trial Tr., at pp. 741:5–742:13 (Cooklev). Based on the evidence presented, no reasonable jury could conclude that a POSITA would not have used LB-031 in conjunction with shared memory.

First, there is no dispute that shared memory, as construed by the Court, was known before these patents were filed. *See id.*, at p. 760:4–11 (Cooklev) ("Q. And you agree that the Mazzoni reference we have looked at discloses shared memory as the term has been construed by the Court for this case; correct? A. I think, yes. Q. And you agree that Mazzoni discloses shared memory that can be allocated between an interleaving function and a deinterleaving function; isn't that correct? A. Yes."); *id.*, at pp. 610:21–611:22 (Jacobsen) (confirming that "shared memory, as the Court has defined it, [was] known prior to the date of TQ Delta's patents" and discussing Mazzoni, Berkman, and Kang); JTX-0056, at 1:59–65 (Mazzoni).

Dr. Jacobsen then explained that there are only two ways of implementing memory for interleaving and deinterleaving in a transceiver—dedicated memory and shared memory. *See* Trial Tr., at pp. 629:25–630:10 (Jacobsen). Thus, although LB-031 is silent as to any specific memory implementation, Dr. Jacobsen testified that, because only two possible options existed, "a person having ordinary skill reading [LB-031] would have understood it to apply to either kind of implementation." *Id.*, at p. 630:7–10; *see also id.*, at p. 642:8–12 ("And again, LB031 does not actually use the words shared memory, but there are only two ways of doing this, either with dedicated memory or with shared memory. And so for the shared memory part, a person having ordinary skill would read it as including shared memory."). Indeed, Dr. Jacobsen confirmed that, at the time LB-031 was contributed to the ITU, there were "discussions on whether to use shared memory . . . once folks realized the breadth of requirements that the service providers had in mind, and the fact that the product might need to be able to do

symmetrical and isometrical [*sic*, asymmetrical] services." *Id.*, at p. 630:11–18 (Jacobsen); *see also id.*, at pp. 634:24–635:3 ("Q. [T]he question was whether the subject of using shared memory and VDSL was being discussed at the standards body meetings around the time of LB031. A. And my recollection is that, yes, it was.").

TQ Delta's only response in the face of this evidence fails because it assumes exactly the thing that it sets out to show, and ignores the unrebutted evidence that shared memory was known in the art at the time of the alleged invention. TQ Delta's expert, Dr. Cooklev, testified that LB-031 would have a certain amount of leftover memory that could not be allocated to an interleaver, or a deinterleaver, as the demands for allocation of memory changed over time. *See* Trial Tr., at pp. 742:14–744:17. He further contended that a certain amount of memory "would be unused," because "when both of these receive[r]s select the smaller of these capabilities, in this case, 10,000 bytes of interleaver memory at the CPE transceiver will just be left unused." *Id.*, at p. 744:8–11. Dr. Cooklev's testimony, however, assumes that there is a certain amount of interleaver memory and a certain amount of deinterleaver memory—that is, that memory is **dedicated** and cannot be allocated to a different function. *See* Trial Tr. at 742:14-744:17; PTX-509 (Cooklev Rebuttal Demonstratives), at pp. 16–17. Dr. Cooklev's testimony fails completely to respond to the combination itself, and ignores his own admission that shared memory was known at the time of the alleged invention. Given the evidence presented at trial, no reasonable jury could have found that the asserted claims were not invalid in view of LB-031 and the knowledge of one of ordinary skill in the art.

2. The Court Should Find The Asserted Claims Obvious In View Of LB-031 And Mazzoni.

The Court should also enter JMOL that the asserted claims are invalid as obvious in view of LB-031 and Mazzoni. TQ Delta disputed only whether a POSITA would have been motivated

to combine LB-031 and Mazzoni, based on the existence of the so-called "Mazzoni problem" raised by Dr. Cooklev. *See* Trial Tr., at pp. 746:19–747:6 (Cooklev). In light of the evidence, no reasonable jury could conclude that a POSITA would not have combined LB-031 with Mazzoni.

Dr. Jacobsen explained at trial why a POSITA would have been motivated to combine the disclosures of LB-031 and Mazzoni:

> Both of these contributions actually refer to trying to manage complexity of an interleaver. And LB-031 says the size of the interleaver memory will be a major source of complexity in VDSL2. And, again, complexity is our little code word for cost.
>
> And the Mazzoni patent says that one of the objects of the invention is to provide a transceiver, a modem architecture that requires a reduced quantity of memory. And specifically aims to significantly reduce the size of the memory means that are used for interleaving and de-interleaving. So the two are aimed at solving the exact same problem in the exact same type of environment, VDSL.

Trial Tr., at pp. 646:24–647:5 (Jacobsen); *see also* JTX-0057, at p. 3 ("The size of the interleaver memory will be a major source of complexity in VDSL2."); JTX-0056, at 1:47–49 ("An object of the invention is to provide a send/receive device (i.e., modem) architecture which requires a reduced quantity of memory."), 2:19–21 ("It is therefore possible to considerably reduce the size of the memory means . . . .").

TQ Delta attempted to challenge Dr. Jacobsen's motivation to combine by raising its manufactured "Mazzoni problem," where, according to Dr. Cooklev, Mazzoni—exactly as written—would not have the amounts of memory required to support the messaging scheme of LB-031. *See* Trial Tr., at pp. 746:19–747:6 (Cooklev). Dr. Jacobsen presented evidence that this purported problem is not actually a problem in two separate ways.

First, Dr. Jacobsen established that a POSITA would not have understood such a problem to even exist. Dr. Jacobsen acknowledged that, based on the disclosure of a set of preconfigured settings in Mazzoni, "it wouldn't work if you just bolted the [LB-031] messaging on to

Mazzoni." Trial Tr., at p. 646:4–5. But, that is not what Dr. Jacobsen proposed, is not what the legal standard requires, and is not what a POSITA would have done. Instead, she explained, "a person having ordinary skill in the art would recognize that that table in Mazzoni is very limiting, and that it would be much more flexible if instead of preconfiguring it, prestoring everything that the transceiver is capable of doing, instead if you negotiated which was common practice in DSL transceivers at the time, that that would result in a much more flexible system." *Id.*, at pp. 645:22–646:3. In other words, Dr. Jacobsen recognized that "[a] person of ordinary skill is also a person of ordinary creativity, not an automaton." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007); *see also ClassCo, Inc. v. Apple, Inc.*, 838 F.3d 1214, 1219 (Fed. Cir. 2016) (upholding Board's finding of motivation to combine and noting that assuming that "a person of ordinary skill in the art can only perform combinations of a puzzle element A with a perfectly fitting puzzle element B" is contrary to law). Dr. Cooklev did not even attempt to rebut Dr. Jacobsen's testimony on this point. To the contrary, rather than recognizing the creativity of a POSITA, he simply took the explicit disclosures of the two references and attempted to "bolt" them together. Only through this improperly narrow view of a POSITA could Dr. Cooklev and TQ Delta construct the "Mazzoni problem."

Second, even assuming that TQ Delta and Dr. Cooklev's "Mazzoni problem" did exist, Dr. Jacobsen testified that a POSITA could, and would be motivated to, solve that problem by adding additional memory to support the LB-031 messaging scheme. *See* Trial Tr., at p. 676:20–24 (Jacobsen). TQ Delta attempted to argue that such a solution would be contrary to the stated purpose of LB-031 and Mazzoni of minimizing the amount of memory, but, as Dr. Jacobsen explained, "the benefit of expanding the memory in any of these references would be that you could support a wider range of services and a higher total bit rate. If you maintained the same size memory and added the messaging scheme you would increase the flexibility of the

approach." *Id.*, at p. 702:6–10. Again, Dr. Cooklev did not dispute Dr. Jacobsen's testimony on her solution to the alleged "Mazzoni problem" or the stated benefits, as recognized by a POSITA, of implementing LB-031's messaging scheme through the use of additional memory.

Accordingly, TQ Delta failed to provide substantial evidence to support the jury's conclusion that a POSITA would not have combined LB-031 and Mazzoni.

C. In The Alternative, The Court Should Grant 2Wire A New Trial.

At a minimum, 2Wire respectfully requests a new trial on the issues of infringement and invalidity because, even if none of the issues raised above would justify JMOL, the jury's verdict is against the clear weight of the evidence, and a new trial must be granted to prevent a miscarriage of justice. *See AVM Techs.*, 334 F. Supp. 3d at 626. In determining whether to grant a new trial, the Court "should consider the overall setting of the trial, the character of the evidence, and the complexity or simplicity of the legal principles which the jury had to apply to the facts." *LG Elecs. U.S.A., Inc. v. Whirlpool Corp.*, 798 F. Supp. 2d 541, 558 (D. Del. 2011).

On the issue of infringement, a new trial is warranted because, as detailed above, TQ Delta and its experts presented the jury with several infringement arguments that were not based upon the actual language of any of the asserted claims: (1) rather than presenting evidence of a message specifying "a maximum number of bytes of memory that are available to be allocated," Dr. Cooklev argued that the message specified the amount of memory "actually being used" by the interleaver or deinterleaver, *see* Trial Tr., at pp. 269:11–270:13 (Cooklev); (2) for the "determining" step, TQ Delta asked the jury to ignore memory that Dr. Yu and Dr. Cooklev testified is required by the Broadcom DSL chips to perform the interleaving and deinterleaving functions, *see id.*, at p. 307:20–22 (Cooklev), despite the fact that the claims recite "determining an amount of memory required by the deinterleaver to deinterleave" and "determining an amount of memory required by the interleaver to interleave"; and (3) for the "allocating" step, TQ Delta

argued that the jury should distinguish between "interleaver memory" and "deinterleaver memory" and "peripheral memory," but those terms are not used in the asserted claims, and, further, TQ Delta's argument is contrary to the plain and ordinary meaning of "memory." Because TQ Delta's infringement theories are unsupported by the asserted claims, the jury's findings as to each of these limitations was against the clear weight of the evidence.

As to invalidity, the Court should grant a new trial because the jury's finding that a POSITA would not be motivated to combine LB-031 with shared memory (either through the knowledge of a POSITA or as disclosed in Mazzoni) was against the clear weight of the evidence. As discussed above, TQ Delta and Dr. Cooklev took a rigid and improperly narrow approach to a POSITA, simply taking the express disclosures of the references and trying to fit them together without applying any level of creativity. *See KSR*, 550 U.S. at 421; *ClassCo*, 838 F.3d at 1219. On the contrary, Dr. Jacobsen explained, for example, that only two types of memories (shared and dedicated) exist and that a POSITA would recognize the benefits of using the LB-031 messaging scheme with shared memory or Mazzoni, and not simply have been "bolting" the references together with no regard for her own common sense and training. *See* Trial Tr., at pp. 645:22–646:3 (Jacobsen). On this record, the jury should have concluded that the asserted claims are invalid, and a new trial is required "to prevent a miscarriage of justice."

IV. CONCLUSION

For the foregoing reasons, 2Wire respectfully requests that the Court enter judgment as a matter of law of non-infringement and invalidity of the asserted claims. In the alternative, the Court should grant 2Wire a new trial on the same issues.

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CERTIFICATE OF SERVICE

I certify that on June 20, 2019, a true and correct copy of the attached document was served on the following counsel by Electronic Mail:

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